CLAIMS:

1. A peripheral bus switch comprising:

a virtual peripheral bus;

a first bridge operably coupled on a first side to the virtual peripheral bus and that supports connection on a second side to a peripheral bus fabric;

a second bridge operably coupled on a first side to the virtual peripheral bus and that supports connection on a second side to the peripheral bus fabric; and

a configurable host bridge operably coupled to the virtual peripheral bus, wherein the configurable host bridge supports a host mode of operation in which it serves as a host bridge, and wherein the configurable host bridge supports a device mode of operation in which it operates as a device.

2. The peripheral bus switch of claim 1, wherein in the host mode of operation the configurable host bridge configures devices of the peripheral bus fabric.

3. The peripheral bus switch of claim 1, wherein in the host mode of operation the configurable host bridge serves as a root bridge of the peripheral bus fabric.

4. The peripheral bus switch of claim 1, wherein in the host mode of operation the virtual peripheral bus serves as a root bus of the peripheral bus fabric.

5. The peripheral bus switch of claim 1, wherein in the device mode of operation:

a root host bridge configures the peripheral bus fabric; and

the configurable host bridge appears to be a peripheral bus device.

6. The peripheral bus switch of claim 5, wherein in the device mode of operation the virtual peripheral bus appears to be a peripheral bus of the peripheral bus fabric.

7. The peripheral bus switch of claim 6, wherein in the device mode of operation the virtual peripheral bus appears to the root host bridge to be a Peripheral Component Interconnect (PCI) bus, a PCI-X bus, a PCI Express bus, or a Hyper Transport bus of the peripheral bus fabric.

8. The peripheral bus switch of claim 1, wherein the virtual peripheral bus, the first bridge, the second bridge, and the configurable host bridge coupled to the virtual peripheral bus are emulated by a system on a chip comprising:

at least one processing unit;

memory;

an internal bus operably coupled to the at least one processing unit and the memory;

a plurality of input ports operably coupled to the internal bus that receive peripheral bus transactions; and

a plurality of output ports operably coupled to the internal bus that transmit peripheral bus transactions.

9. The peripheral bus switch of claim 1, wherein the configurable host bridge shares a memory space with at least one other host bridge coupled via the peripheral bus fabric.

10. The peripheral bus switch of claim 1, wherein:

at least a portion of the peripheral bus fabric supports at least one version of the HyperTransport™ specification; and

the virtual peripheral bus appears to support one or more versions of the Peripheral Component Interconnect (PCI) specification, the PCI-X specification, or the PCI Express specification.

11. A processing device that emulates a peripheral bus switch, the processing device comprising:

at least one processing unit;

memory;

an internal bus operably coupled to the at least one processing unit and the memory;

a plurality of input ports operably coupled to the internal bus that receive peripheral bus transactions; and

a plurality of output ports operably coupled to the internal bus that transmit peripheral bus transactions.

wherein the at least one processing unit executes a plurality of instructions to cause the processing device to emulate:

a virtual peripheral bus;

a first bridge operably coupled on a first side to the virtual peripheral bus and that supports connection on a second side to a peripheral bus fabric;

a second bridge operably coupled on a first side to the virtual peripheral bus and that supports connection on a second side to the peripheral bus fabric; and

a configurable host bridge operably coupled to the virtual peripheral bus, wherein the configurable host bridge supports a host mode of operation in which it serves as a host bridge, and wherein the configurable host bridge supports a device mode of operation in which it operates as a device.

12. The processing device of claim 11, wherein in the host mode of operation the emulated configurable host bridge configures devices of the peripheral bus fabric.

13. The processing device of claim 11, wherein in the host mode of operation the emulated configurable host bridge serves as a root bridge of the peripheral bus fabric.

14. The processing device of claim 11, wherein in the host mode of operation the emulated virtual peripheral bus serves as a root bus of the peripheral bus fabric.

15. The processing device of claim 11, wherein in the device mode of operation:

a root host bridge configures the peripheral bus fabric; and

the emulated configurable host bridge appears to be a peripheral bus device.

16. The processing device of claim 15, wherein in the device mode of operation the emulated virtual peripheral bus appears to be a peripheral bus of the peripheral bus fabric.

17. The processing device of claim 16, wherein in the device mode of operation the emulated virtual peripheral bus appears to the root host bridge to be a Peripheral Component Interconnect (PCI) bus, a PCI-X bus, a PCI Express bus, or a Hyper Transport bus of the peripheral bus fabric.

18. The processing device of claim 11, wherein at least some of the components of the processing device share a memory space with at least one other host bridge coupled via the peripheral bus fabric.

19. The processing device of claim 11, wherein:

at least a portion of the peripheral bus fabric supports at least one version of the Hyper Transport specification; and

the emulated virtual peripheral bus appears to support one or more versions of the Peripheral Component Interconnect (PCI) specification, the PCI-X specification, or the PCI Express specification.

20. In a processing device having at least one processing unit, memory, an internal bus operably coupled to the at least one processing unit and to the memory, a plurality of input ports operably coupled to the internal bus, and a plurality of output ports operably coupled to the internal bus, a method for supporting peripheral bus switch operations comprising:

emulating a virtual peripheral bus;

bridging input peripheral bus transactions received on the plurality of input ports to the emulated virtual peripheral bus;

bridging output peripheral bus transactions from the emulated virtual input peripheral bus to the plurality of output ports;

emulating a host bridge that is operably coupled to the virtual peripheral bus;

in a host mode of operation, the configurable host bridge operating as a host bridge on the virtual peripheral bus; and

in a device mode of operation, the configurable host bridge operating as a device on the virtual peripheral bus.

21. The method of operation of claim 20, further comprising, in the host mode of operation, the configurable host bridge configuring devices of the peripheral bus fabric.

22. The method of operation of claim 20, further comprising, in the host mode of operation, the configurable host bridge serving as a root bridge of the peripheral bus fabric.

23. The method of operation of claim 20, further comprising, in the host mode of operation, the virtual peripheral bus serving as a root bus of the peripheral bus fabric.

24. The method of operation of claim 20, further comprising, in the host mode of operation:

a root host bridge configuring the peripheral bus fabric; and

the configurable host bridge acting as a peripheral bus device on the virtual peripheral bus.

25. The method of operation of claim 24, further comprising, in the device mode of operation, the virtual peripheral bus appearing to be a peripheral bus of the peripheral bus fabric.

26. The method of operation of claim 25, further comprising, in the device mode of operation, the virtual peripheral bus appearing to the root host bridge to be a Peripheral Component Interconnect (PCI) bus, a PCI-X bus, a PCI Express bus, or a Hyper Transport bus of the peripheral bus fabric.

27. The method of operation of claim 20, further comprising the configurable host bridge sharing a memory space with at least one other host bridge coupled via the peripheral bus fabric.